under 35 U.S.C. §112, second paragraph. In response, the applicants have amended the claims to remove the antecedent basis rejections.

In the office action, the Examiner rejected claims 1 and 5 under 35 U.S.C. §102 over U.S. Patent No. 6,084,880 to Bailey et al. (hereinafter "Bailey"). The Examiner identifies column 15, lines 27-41 as teaching "issuing an instruction to disable interrupts for a period of time specified in the instruction" and equates this quotation with the language of claim 1.

The applicants agree with the Examiner that Bailey teaches disabling interrupts for a period of time in the quoted portion. However, Bailey does not teach or suggest fetching an interrupt disable instruction, nor fetching an interrupt disable instruction where the instruction specifies a number of cycles for disabling interrupt processing, nor executing the instruction, all as claimed. Rather, the interrupt disable feature described in Bailey is one that is used reactively by the host, when interrupts received are numerous, by setting a timer. (Bailey, 15:27-29). Bailey therefore does not teach or suggest an interrupt disable instruction designed to be fetched from a program sequence, nor does Bailey teach or suggest an operand in such an instruction that identifies a number of processor cycles for a delay or executing that instruction. For these reasons, Bailey does not anticipate or render obvious independent claim 1 or claims depending therefrom.

With respect to dependent claim 5, for the same reasons described above, while Bailey does teach a timer, Bailey does not teach fetching an interrupt disable instruction or executing that instruction to disable the interrupt for a particular number of processor cycles as required by claim 5.

The Examiner rejects the remaining claims under 35 U.S.C. §103 over combinations of Bailey with U.S. Patent No. 6,181,151 to Wasson, U.S. Patent No. 5,826,072 to Knapp et al.

("Knapp") and a definition of "register" in the Microsoft Computer Dictionary. The Examiner indicates that Wasson teaches a test instruction but not an interrupt disable instruction. The Examiner indicates that Knapp teaches an instruction with a pointer that points to a memory location containing an operand that the instruction is intended to operate on. Knapp does not teach or suggest, however, an interrupt disable instruction. In addition, the Microsoft definition of register cited by the Examiner does not teach or suggest an interrupt disable instruction. Therefore, an interrupt disable instruction required by independent claims 1 and 14 is not found in the prior art through any combination of references cited, and a prima facie case of obviousness is thus not made by the examiner. Furthermore, because an interrupt disable instruction is not taught in the prior art, many of the other claim features are missing, including storing the interrupt disable instruction in a program memory, as required by independent claim 14 and claims depending therefrom.

Because the prior art alone and in combination fails to teach the claimed invention embodied in independent claims 1 and 14, and claims depending therefrom, applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner has any questions about this Amendment and to facilitate prosecution, the Examiner is encouraged to call the undersigned attorney.

Respectfully submitted,

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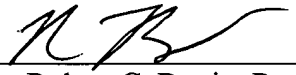
Dated: April 22, 2004

By: 

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